CERN Openlab

First benchmarks on Intel's new Sandy Bridge (desktop) processor

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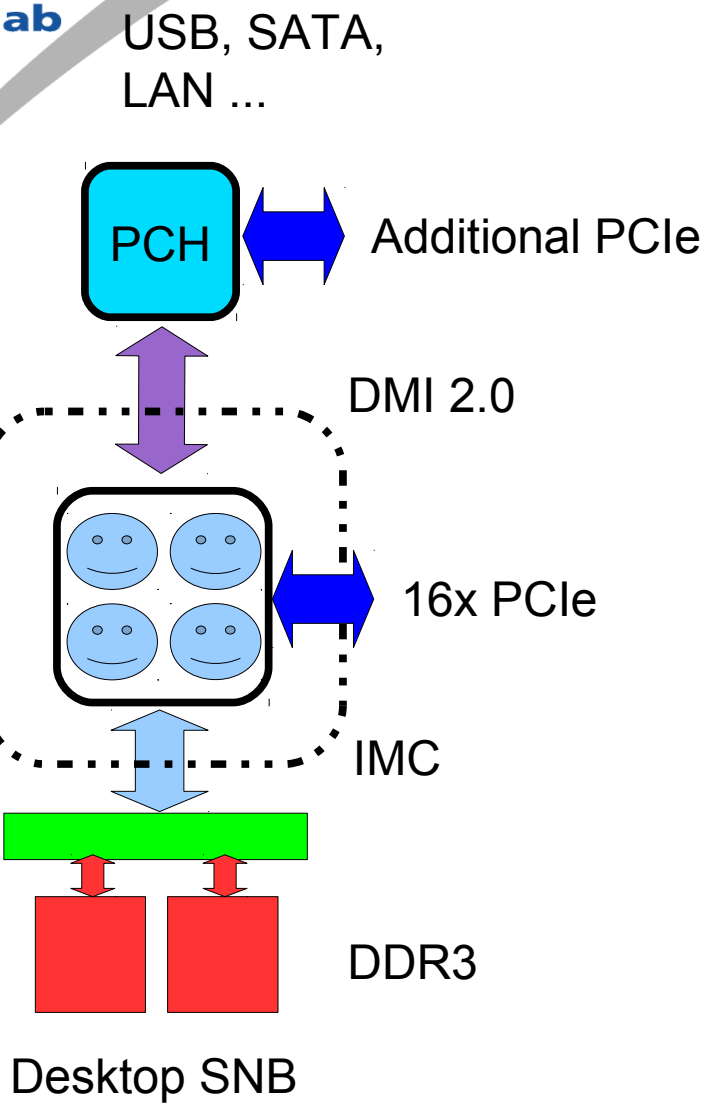
Sandy Bridge Microarchitecture

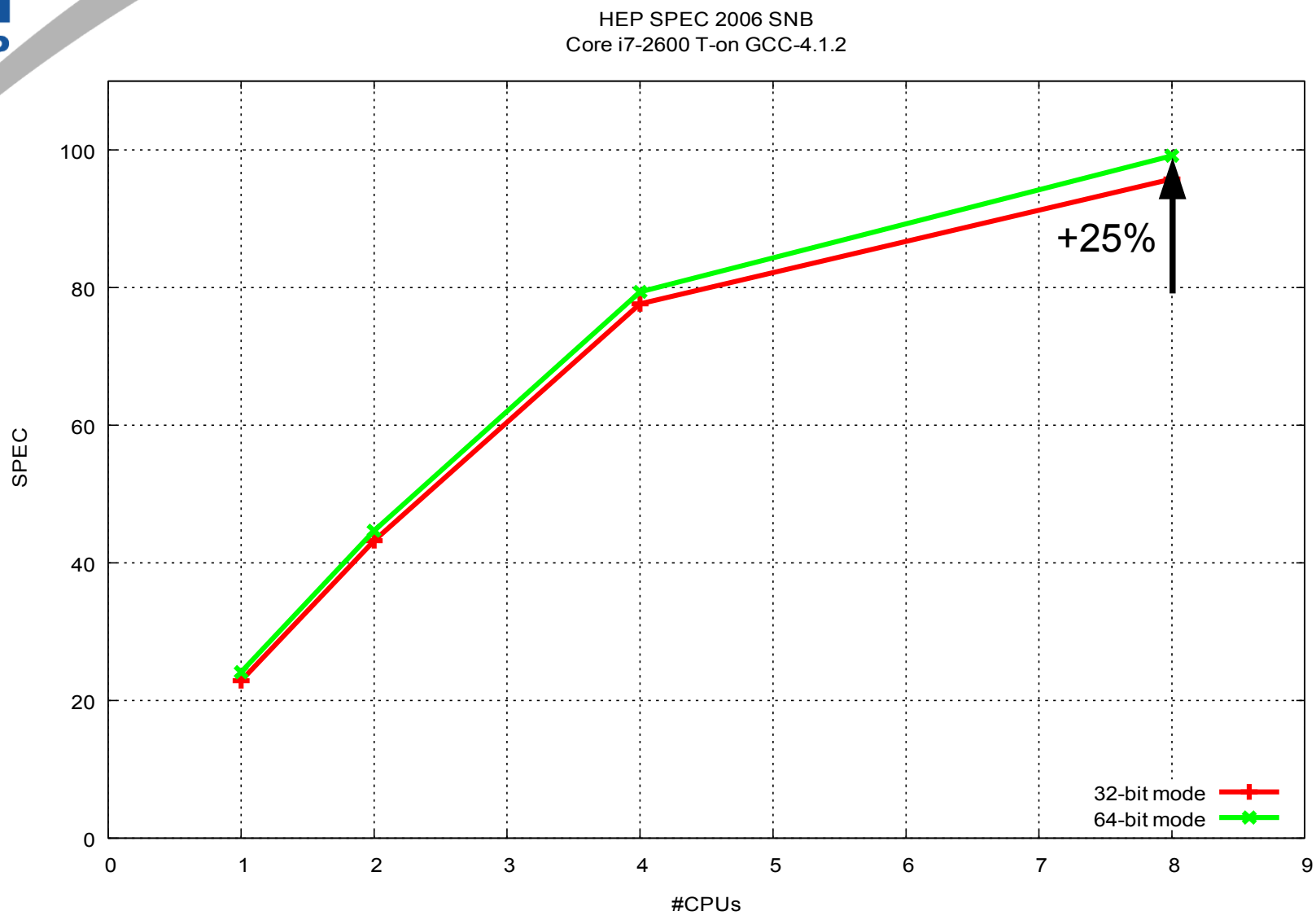
- Second generation Core processor family
- Integrated memory controller
- Integrated PCIe bus
- AVX vector instructions
  - 256 bit long vectors doubling SSE vector width
- On die GPU for desktop parts
- Improved Turbo
  - For the cores and the GPU
- SMT

Sandy Bridge Microarchitecture

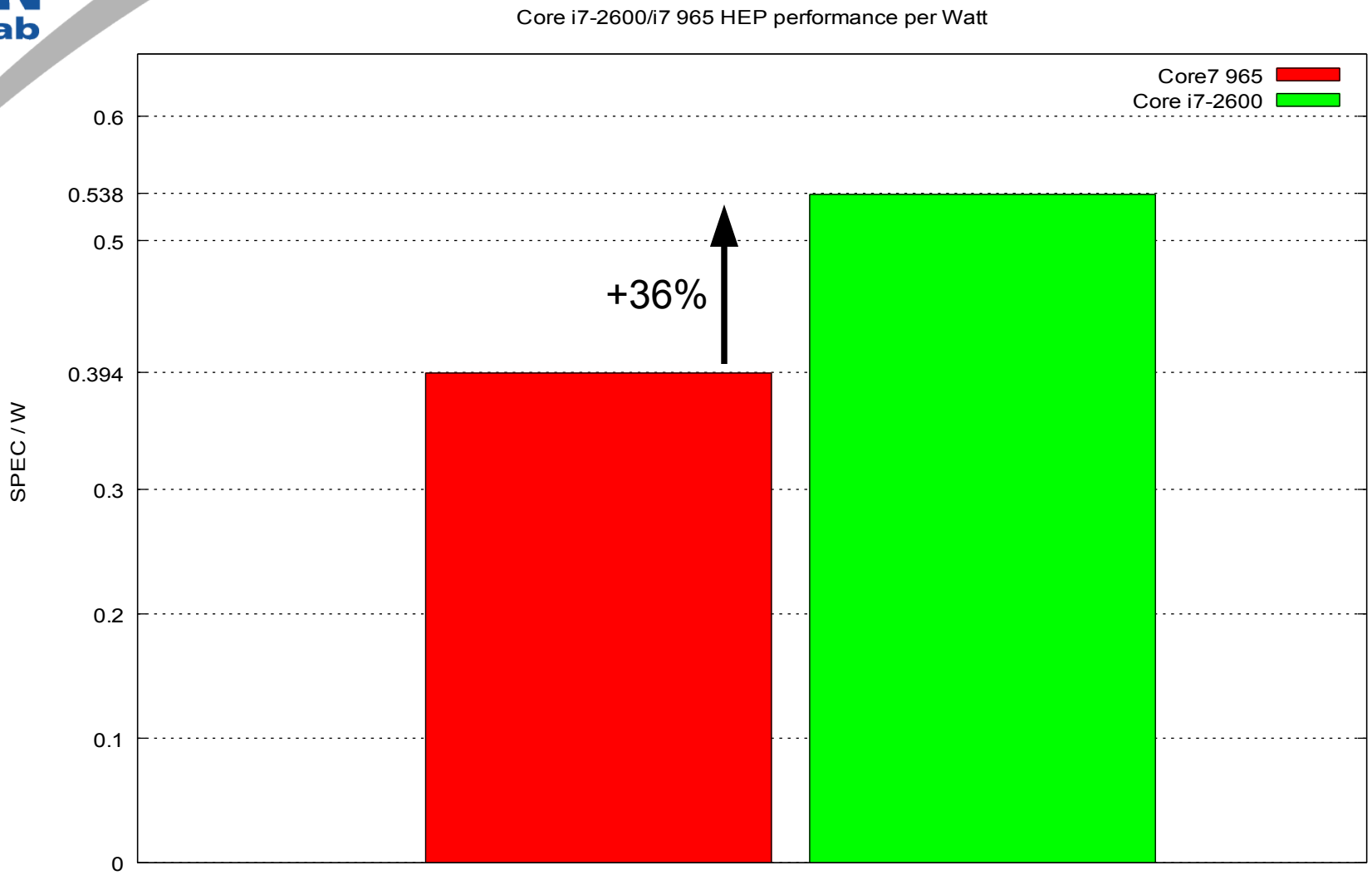


- Core i7-2600 @3.4GHz (3.8GHz max Turbo)
- 2 memory channels
- New LGA1155 socket
- Direct Media Interface 2.0 (20Gb/s) to Platform Controller Hub

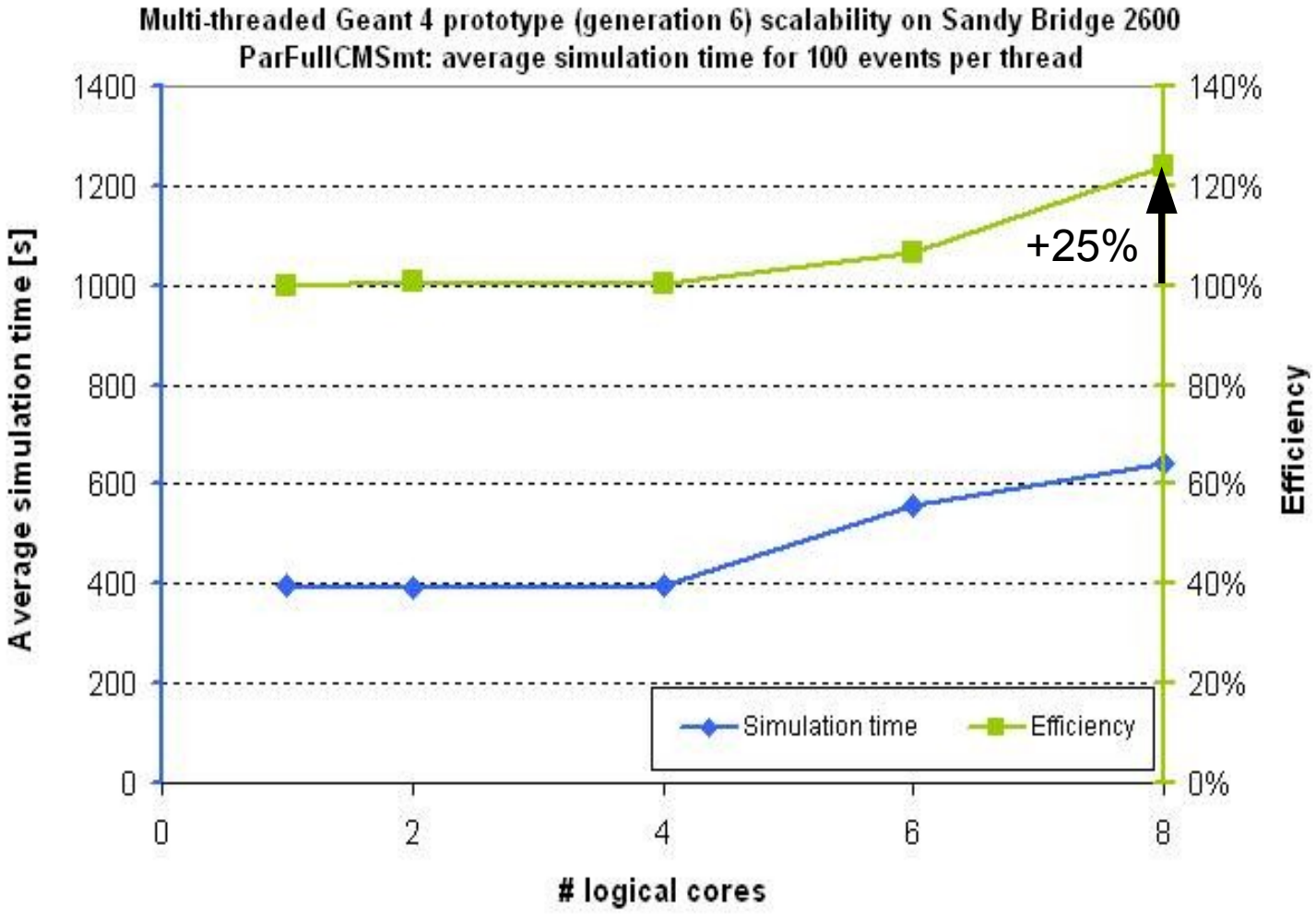
HEPSPEC mesurements



HEPSPEC measurements



Multi-threaded Geant4



Multi-threaded Geant4

CPU / Conf	Events / thread	1	2	4	6	8
"Sandy Bridge" i7-2600, SLC6, 4 cores, 8 threads, gcc 4.3.4, 64-bit, 12 GB memory (opladev34) 100 evts per thread	100	0.2521 (110.2%)	0.2538 (110.1%)	0.2528 (111.0%)	0.1792 (78.0%)	0.1563 (67.9%)
"Westmere-EP" L5640, SLC5, 12 cores, 24 threads, gcc 4.3.4, 64-bit, 12 GB memory (opladev32) 100 evts per thread	100	0.1528 (100.0%)	0.1539 (100.0%)	0.1521 (100.0%)	0.1534 (100.0%)	0.1536 (100.0%)

- SMT increases throughput by 24%
- At the same frequency, a Sandy Bridge core is 10% faster than a Westmere core

Advanced Vector Extensions

- Available starting with Sandy Bridge
  - AVX doubled vector floating point performance
  - No integer operations yet
  - Mixing SSE and AVX has a cost
- High Level Trigger benchmark initial port to AVX using intrinsics
  - Fit time per track (lower is better):

    SSE PD: 0.84 us
    SSE PS: 0.37 us
    AVX PD: 0.66 us
    AVX PS: 0.29 us
  - Porting SSE code using AVX intrinsics was easy
  - Still needs investigations to fully benefit from the longer vectors

Conclusion

- A lot of investigations are still to be conducted
- AVX support is still limited
  - Recent linux kernels
  - ICC
  - GCC 4.6 snapshots
- Performance monitoring tools for Sandy Bridge difficult to use as a standard user